CLAIMS

What is claimed are:

1. A method of manufacturing a semiconductor device, comprising the steps of:

providing a semiconductor substrate in which a cell region and a peripheral circuit region are defined;

forming a patterned tunnel oxide film, a floating gate electrode and a control gate electrode in said cell region forming a gate electrode in said peripheral circuit region;

removing an exposed portion of a device isolation film in said cell region by means of a self align source etch process;

forming a first capping layer and a second capping layer on the entire structure;

performing a self align source annealing process for said cell region;

forming a source and drain junction in said cell region and forming a low concentration source and drain junction in said peripheral circuit region;

forming a gate spacer in said peripheral circuit region; and

forming a high concentration source and drain junction in said peripheral circuit region.

2. The method of manufacturing a semiconductor device according to claim 1, wherein said first capping layer is formed in thickness of 100 ~

200Å.

3. The method of manufacturing a semiconductor device according to claim 1, wherein said second capping layer is formed in thickness of 50 ~ 150Å.

4. The method of manufacturing semiconductor devices according to claim 1, wherein said gate spacer is formed of said first capping layer/said second capping layer/an oxide film for a spacer in a way that an oxide film for a spacer is formed on said second capping layer and said oxide film for a spacer and said second capping layer are then sequentially etched by a blanket etch process.

5. The method of manufacturing semiconductor devices according to claim 4, wherein said oxide film for a spacer is formed in thickness of 1200 ~ 1600Å.

6. The method of manufacturing semiconductor devices according to claim 4, wherein said oxide film for a spacer and said first capping layer are etched through the mediation of said second capping layer to form a screen oxide film.

7. The method of manufacturing semiconductor devices according to claim 1, wherein said source and drain junction in said cell region is formed

by using said first capping layer and said second capping layer as an ion implantation screen oxide film.

8. The method of manufacturing semiconductor devices according to claim 1, wherein said low concentration source and drain junction in said peripheral circuit region is formed by using said first capping layer and said second capping layer as an ion implantation screen oxide film.

9. The method of manufacturing semiconductor devices according to claim 1, wherein said high concentration source and drain junction in said peripheral circuit region is formed by using said first capping layer etched by a given thickness as an ion implantation screen oxide film.

10. The method of manufacturing semiconductor devices according to claim 1, wherein said first capping and said second capping layer functions to prohibit a local bird's beak of said dielectric film formed between said floating gate electrode and said control gate electrode.